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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,476	08/30/2001	Cliff Zitlaw	400.125US01	9314

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EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,476	ZITLAW, CLIFF	
	Examiner	Art Unit	
	Woo H. Choi	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 3, 5, 11, 12, 15, 18 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Baltz (US Patent No. 6,058,474, hereinafter "Baltz").

3. With respect to claims 1 and 21, Baltz discloses a processing system (figure 8) comprising:

a processor (10);

a volatile memory device (23 and 100) coupled to communicate with the processor; and

a non-volatile memory device (671) coupled to the processor and connected to the volatile memory device, wherein the non-volatile memory device transfers data directly to the volatile memory device during power-up without intervention by any other device (col. 7, lines 46 – 60, see also abstract).

4. With respect to claim 2, the volatile memory device initiates the data transfer in response to a reset signal (abstract).

5. With respect to claim 3, the volatile memory device provides a system reset signal to the processor after the data is transferred from the non-volatile memory device (col. 7, lines 56 – 60).

6. With respect to claim 5, the volatile memory device initiates the data transfer in response to a reset signal provided by an external reset controller (figures 1A, 4A, 7, 8, reset signal 76 comes from an external source).

7. With respect to claim 11, Baltz discloses a processor system power-up method comprising:

detecting a power-up condition and providing a reset signal to a synchronous memory (abstract and col. 1, lines 25 – 29);

initiating a direct data transfer from a non-volatile memory to the synchronous memory, without intervention from any other device, in response to the reset signal (abstract); and

providing a system reset signal from the synchronous memory to a processor upon completion of the direct data transfer (col. 7, lines 56 – 60).

8. With respect to claims 12, the synchronous memory device is an SDRAM (col. 6, lines 7 – 8).

9. With respect to claim 15, the method further comprises loading the non-volatile memory with the processor prior to detecting the power-up condition (figure 8, 671, EPROM is loaded with a boot code prior to the power-up).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 4, 6 – 9, 14, 16 – 19, rejected under 35 U.S.C. 103(a) as being unpatentable over Baltz in view of Harari *et al.*(US Patent No. 6,266,724, hereinafter "Harari").

Baltz discloses a method of improving a processor system power-up comprising:

detecting a power-up condition with a reset controller and providing a reset signal to an SDRAM;

using the SDRAM, initiating a direct data transfer from an EPROM memory to the SDRAM, over a dedicated bus (figure 8, bus 73 appears to be dedicated for direct transfer of data from memories) in response to the reset signal via a bus without intervention by any other device; and

providing a system reset signal from the SDRAM to a processor after the data has been transferred (see the rejections above).

However, Baltz does not specifically disclose the use of a flash memory for non-volatile memory coupled via a serial bus. On the other hand, Harari discloses a processor system that loads data from a flash memory (figure 7) via a serial bus (col. 7, Lines 34 – 36).

It would have been obvious to one of ordinary skill in the art, having the teachings of Baltz and Harari before him at the time the invention was made, to use the flash memory and decompression teachings of the computer system that loads data from a flash EPROM of Harari in the computer system that loads data from an EPROM of Baltz, in order to provide a removable PC card that can accommodate components offloaded from the host system to minimize the size and cost of the host system and to provide flexibility in system configuration (Harari, col. 3, 31 – 35).

12. With respect to claims 18, the synchronous memory device is an SDRAM (col. 6, lines 7 – 8).

13. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baltz in view of Shin (US Patent No. 6,735,669).

Baltz discloses all of the limitations of the parent claim as discussed above. However, Baltz does not specifically disclose the use of a RDRAM. On the other hand Shin discloses that

a RDRAM has various operational modes for low power system operation (Shin, col. 1, lines 16 – 20).

It would have been obvious to one of ordinary skill in the art, having the teachings of Baltz and Shin before him at the time the invention was made, to use the lower power consumption RDRAM teachings of Shin in the computer system of Baltz, in order to reduce the overall system power consumption. Reduce power consumption is especially important in battery operated portable computer systems.

14. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baltz in view of Harari as applied to clams 6 and 19 and further in view of Shin.

Baltz and Harati disclose all of the limitations of claims 6 and 19 as discussed above. However, Baltz and Harati do not specifically disclose the use of a RDRAM. On the other hand Shin discloses that a RDRAM has various operational modes for low power system operation (Shin, col. 1, lines 16 – 20).

It would have been obvious to one of ordinary skill in the art, having the teachings of Baltz, Harati and Shin before him at the time the invention was made, to use the lower power consumption RDRAM teachings of Shin in the computer system of Baltz and Harati, in order to reduce the overall system power consumption. Reduce power consumption is especially important in battery operated portable computer systems.

Response to Arguments

17. Applicant's arguments, see Response to Non-Final Office Action, filed May 19, 2005, with respect to rejections of claims 6, 16, 19, and 20 under 35 U.S.C. 112, first paragraph have been fully considered and are persuasive. The corresponding rejections of claims 6, 16, 19 and 20 have been withdrawn.

18. Applicant's arguments filed May 19, 2005, have been fully considered but they are not persuasive. The DMA controller DMA0 100 is clearly identified as being a part of the volatile memory device in the rejection. The claim requires that there be no intervention by any **other** device. Moreover, in a DMA transfer, the data transfer is **direct** between the devices involved. The DMA controller sets up the transfer and controls the transfer but does not intervene. Applicant's argument that "[t]here is no control or intervention used in the transfer of data in the processing system of the present invention as claimed" is absurd as every memory device requires associated control circuitries. Applicant's argument that direct transfer does not necessarily imply "without intervention" is contradicted by Applicant's argument that the limitation "without intervention" is supported by the statement "[t]he present invention allows the non-volatile memory contents to be **directly** loaded into the SDRAM without intervention by the processor" found in the specification. The limitation "without intervention by **any other device**" is not supported by the disclosure "without intervention by **the processor.**" The only other source of support for the claimed limitation then is the **direct** loading between devices. If direct loading does not imply "without intervention" as Applicant argues, then the claimed

argues, then the claimed limitations are not supported by the application as originally filed and therefore, subject to rejections under 35 U.S.C. 112, first paragraph.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

whc
July 7, 2005

BEHZAD JAMES PEIKARI
PRIMARY EXAMINER